What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate;

a semiconductor element formed on said semiconductor substrate by overlaying a plurality of patterned layers; and

a position check mark used for overlay of said plurality of layers,

wherein said semiconductor element includes:

an interlayer insulating film formed on said semiconductor substrate;

a contact hole penetrating said interlayer insulating film to reach said semiconductor substrate;

a plug that is conductive and fills said contact hole;

a barrier metal layer provided to cover said contact hole and to be electrically connected to said plug; and

a conductive film formed on said barrier metal layer,

and wherein said position check mark includes:

a plurality of mark holes formed to penetrate said interlayer insulating film;

a recess plug that is conductive and provided so that its one end portion on a side opposite to said semiconductor substrate is recessed in said plurality of mark holes;

and wherein said barrier metal layer is provided to cover said plurality of mark holes and to be electrically connected to said recess plug; and

said conductive film is formed on said barrier metal layer.

2. The semiconductor device according to claim 1, wherein

an opening size of each of said plurality of mark holes ranges from almost as large as an opening size of said contact hole to almost twice as large as the opening size of said contact hole.

3. The semiconductor device according to claim 1, wherein

said plurality of mark holes are formed through a same process as said contact hole.

4. A semiconductor device, comprising:

a semiconductor substrate;

a semiconductor element formed on said semiconductor substrate by overlaying a plurality of patterned layers; and

a position check mark used for overlay of said plurality of layers,

wherein said semiconductor element includes:

an interlayer insulating film formed on said semiconductor substrate;

a contact hole penetrating said interlayer insulating film to reach said semiconductor substrate;

a plug that is conductive and fills said contact hole;

a barrier metal layer provided to cover said contact hole and to be electrically connected to said plug; and

a conductive film formed on said barrier metal layer,

and wherein

said position check mark has a recess region in which a determined region of said interlayer insulating film is recessed;

a plurality of mark holes are formed to penetrate said interlayer insulating film in said recess region;

a protrusion plug that is conductive is provided so that its one end portion on a side opposite to said semiconductor substrate protrudes from said plurality of mark holes;

said barrier metal layer is provided to cover said plurality of mark holes and to be electrically connected to said protrusion plug; and

said conductive film is formed on said barrier metal layer.

5. The semiconductor device according to claim 4, wherein

an opening size of each of said plurality of mark holes ranges from almost as large as an opening size of said contact hole to almost twice as large as the opening size of said contact hole.

6. The semiconductor device according to claim 4, wherein

said plurality of mark holes are formed through a same process as said contact hole.

7. A method of manufacturing a semiconductor device that includes a semiconductor element formed on a semiconductor substrate by overlaying a plurality of patterned layers and a position check mark for overlay of said plurality of layers,

said method comprising:

(a) forming a first wiring layer on a first region in which said semiconductor element is formed on said semiconductor substrate and a second region that surrounds said first region with an insulating film interposed therebetween;

(b) forming an upper oxide film and a sidewall oxide film in an upper portion and on a side surface of said first wiring layer, respectively;

(c) forming a nitride film to cover said upper oxide film and said sidewall oxide film;

(d) forming an interlayer insulating film to cover said first and second regions;

(e) forming a contact hole in a self-aligned manner to penetrate said interlayer insulating film of said first region to reach at least said nitride film extending from on said sidewall oxide film to on said semiconductor substrate, and selectively removing said interlayer insulating film of said second region in accordance with a formation region of said position check mark to form an opening, thereby exposing said nitride film;

(f) removing said nitride film exposing a bottom of said contact hole and said opening to extend said contact hole to said semiconductor substrate and to leave a mark structure of said insulating film, said first wiring layer, said upper oxide film, and said side wall oxide film formed in said opening in said steps (a) and (b); and

(g) forming a second wiring layer to cover said first and second regions, burying said second wiring layer in said contact hole, and placing said second wiring layer along an outline of said mark structure at a same time,

wherein said position check mark is formed in said steps (f) and (g).

8. The method according to claim 7, wherein

said step (d) of forming said interlayer insulating film includes a step of planarizing said interlayer insulating film by CMP (Chemical Mechanical Polishing).

9. A method of manufacturing a semiconductor device that includes a semiconductor element formed on a semiconductor substrate by overlaying a plurality of patterned layers and a position check mark used for overlay of said plurality of layers,

said method comprising:

(a) forming a first wiring layer on a first region in which said semiconductor element is formed on said semiconductor substrate and a second region that surrounds said first region with an insulating film interposed therebetween;

(b) forming an upper oxide film in an upper portion of said first wiring layer;

(c) forming a sidewall oxide film on side surfaces of said first wiring layer and said upper oxide film in said first region;

(d) forming a nitride film to cover said upper oxide film and said sidewall oxide film in said first region and said first wiring layer and said upper oxide film in said second region;

(e) selectively removing said nitride film covering said first wiring layer and said upper oxide film in said second region to form a sidewall nitride film;

(f) forming an interlayer insulating film to cover said first and second regions;

(g) forming a contact hole in a self-aligned manner to penetrate said interlayer insulating film of said first region to reach at least said nitride film extending from on said sidewall oxide film to on said semiconductor substrate, selectively removing said interlayer insulating film of said second region in accordance with a formation region of said position check mark to provide an opening, exposing said nitride film, and removing said upper oxide film;

(h) removing said nitride film exposing a bottom of said contact hole and said opening to extend said contact hole to said semiconductor substrate and to leave a mark

structure of said insulating film, said first wiring layer, and said side wall nitride film formed in said opening in said steps (a), (b), and (e); and

(i) forming a second wiring layer to cover said first and second regions, burying said second wiring layer in said contact hole, and placing said second wiring layer along an outline of said mark structure exposed in said opening at a same time,

wherein said position check mark is formed in said steps (h) and (i).

10. The method according to claim 9, wherein

said step (f) of forming said interlayer insulating film includes a step of planarizing said interlayer insulating film by CMP (Chemical Mechanical Polishing).

11. A method of manufacturing a semiconductor device that includes a semiconductor element formed on a semiconductor substrate by overlaying a plurality of patterned layers and a position check mark used for overlay of said plurality of layers,

said method comprising:

(a) forming an interlayer insulating film to cover a first region in which said semiconductor element is formed on said semiconductor substrate and a second region that surrounds said first region;

(b) providing a contact hole that penetrates said interlayer insulating film of said first region to reach said semiconductor substrate, and forming a plurality of mark holes that penetrate said interlayer insulating film of said second region to reach said semiconductor substrate;

(c) forming a conductive film on said interlayer insulating film on said first and second regions to fill said contact hole and said plurality of mark holes;

(d) forming an insulating film on said conductive film;

(e) selectively removing said insulating film and said conductive film to leave said insulating film on said contact hole and leave said conductive film on said plurality of mark holes and between said plurality of mark holes;

(f) forming sidewalls that are conductive on side surfaces of said conductive film and said insulating film on said contact hole and side surfaces of said conductive film and said insulating film on said plurality of mark holes and between said plurality of mark holes; and

(g) removing said insulating film, wherein said position check mark is formed in said steps (b) to (g).

12. The method according to claim 11, wherein

said step (b) includes a step of setting an opening size of each of said plurality of mark holes to range from almost as large as an opening size of said contact hole to almost twice as large as the opening size of said contact hole.

13. The method according to claim 11, wherein

said step (a) of forming said interlayer insulating film includes a step of planarizing said interlayer insulating film by CMP (Chemical Mechanical Polishing).

14. A method of manufacturing a semiconductor device that includes a semiconductor element formed on a semiconductor substrate by overlaying a plurality of patterned layers and a position check mark used for overlay of said plurality of layers,

said method comprising:

(a) forming an interlayer insulating film to cover a first region in which said semiconductor element is formed on said semiconductor substrate and a second region that surrounds said first region;

(b) providing a contact hole that penetrates said interlayer insulating film of said first region to reach said semiconductor substrate, and forming a plurality of mark holes that penetrate said interlayer insulating film of said second region to reach said semiconductor substrate;

(c) filling said contact hole and said plurality of mark holes with a plug that is conductive;

(d) partially removing said plug so that one end portion of said plug in said plurality of mark holes on a side opposite to said semiconductor substrate is recessed in said plurality of mark holes, to form a recess plug; and

(e) placing a barrier metal layer to cover said first and second regions and to be electrically connected to said plug in said contact hole and said recess plug in said plurality of mark holes, and then forming a conductive film on said barrier metal layer,

where said position check mark is formed in said steps (b) to (c).

15. The method according to claim 14, wherein

said step (b) includes a step of setting an opening size of each of said plurality of mark holes to range from almost as large as an opening size of said contact hole to almost twice as large as the opening size of said contact hole.

16. The method according to claim 14, wherein

said step (a) of forming said interlayer insulating film includes a step of planarizing said interlayer insulating film by CMP (Chemical Mechanical Polishing).

17. A method of manufacturing a semiconductor device that includes a semiconductor element formed on a semiconductor substrate by overlaying a plurality of patterned layers and a position check mark used for overlay of said plurality of layers,

said method comprising:

(a) forming an interlayer insulating film to cover a first region in which said semiconductor element is formed on said semiconductor substrate and a second region that surrounds said first region;

(b) providing a contact hole that penetrates said interlayer insulating film of said first region to reach said semiconductor substrate, and forming a plurality of mark holes that penetrate said interlayer insulating film of said second region to reach said semiconductor substrate;

(c) filling said contact hole and said plurality of mark holes with a plug that is conductive;

(d) recessing a predetermined region in said interlayer insulating film of said second region to which said plurality of mark holes are formed to form a recess region and protruding one end portion of said plug on a side opposite to said semiconductor substrate from said plurality of mark holes, to form a protrusion plug; and

(e) placing a barrier metal layer to cover said first and second regions and to be electrically connected to said plug in said contact hole and said protrusion plug protruding from said plurality of mark holes, and then forming a conductive film on said barrier metal layer,

wherein said position check mark is formed in said steps (b) to (e).

18. The method according to claim 17, wherein

said step (b) includes a step of setting an opening size of each of said plurality of mark holes to range from almost as large as an opening size of said contact hole to almost twice as large as the opening size of said contact hole.

19. The method according to claim 17, wherein

said step (a) of forming said interlayer insulating film includes a step of planarizing said interlayer insulating film by CMP (Chemical Mechanical Polishing).